# A SIMPLE CMOS POWER CONTROL CIRCUIT FOR THE HMC408LP3 AMPLIFIER

## General Description

The HMC408LP3 is a 5.1 - 5.9 GHz high efficiency GaAs InGaP Heterojunction Bipolar Transistor (HBT) Power Amplifier MMIC, which offers +30 dBm P1dB. The amplifier provides 20 dB of gain, +32.5 dBm of saturated power, and 27% PAE from a single +5.0 V supply voltage. The input is internally matched to 50 Ω while the output requires a minimum of external components. Vpd can be used for full power down or RF output power/current control. The amplifier is packaged in a low cost, 3 x 3 mm leadless surface mount package with an exposed base for improved RF and thermal performance.

## Application Problem

The HMC408LP3 power amplifier is designed to meet the requirements of today's 802.11a and UNII communication equipment. Advancements in the semiconductor industry have allowed for smaller products with increased functionality to flourish in the marketplace. With these enhancements comes a pressure to reduce the power consumption of the devices in order to preserve battery life and minimize thermal dissipation. For this reason, the majority of devices now incorporate some type of power control or efficiency control. The HMC408LP3 meets these requirements by allowing the user to control the output power and current of the power amplifier by varying a voltage on a control pin (VPD). For maximum operating power, (31.0 dBm saturated power @5.5 GHz), the control pin requires 5 V with a minimum of 14 mA of current. This current drive requirement will present a problem to certain logic gate families[1]. To solve this problem, a load switch is implemented in the VPD control path of the power amplifier. The implementation of the load switch makes the power amplifier compatible to all logic gates.

## Application Solution

Figure 1 shows a load switch, which consists of two MOSFET transistors, one P-channel, the other N-channel. Application of a logic "high" to the gate of Q2 will turn the device on and as a result apply a ground to the gate of Q1, turning it on. A logic "low" turns off Q2, causing resistor R1 to pull the gate of Q1 up to the input voltage, subsequently turning Q1 off. When Q1 and Q2 are on, resistors R1 and R2 will provide a current path to ground. To minimize this leakage current the values of R1 and R2 should be chosen using the equation (1):

$$I_{leakage} = \frac{Vin}{R1 + R2} \quad (1)$$

Where Vin is the input voltage to Q1 and the value of R1 is at least 10 times smaller than R1 to insure that Q2 will turn on.

In addition, large decoupling capacitors on the output should be avoided. For example, a 100 uF capacitor could theoretically cause a 30 A transient current during turn-on, which could stress the voltage source. These current spikes are dampened by either increasing the value of R1 or applying a capacitor (C12) across the gate and drain of Q1. For this application, the value of the decoupling capacitor is low enough to minimize any current spikes.

The rise / fall time of the HMC408LP3, which is typically 50 nS, will change with the addition of the load switch. The two components, which most effect the rise / fall time, are resistors R2 and R1. R1 effects the fall time while R2 will effect the rise time. To decrease rise / fall time, these values need to be lowered which will increase the leakage current. Naturally, a compromise must be made between rise / fall time and leakage current.

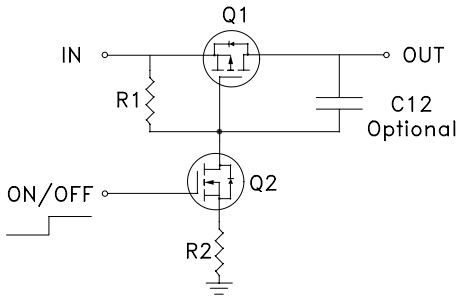


**Figure 1** - Dual MOSFET load switch

## Application Circuit

A load switch is implemented on the VPD line of the HMC408LP3 as shown in figure 2. Instead of using discrete MOSFETS, an integrated IC containing both MOSFETS is used. The integrated IC is the FDC6323L manufactured by Fairchild Semiconductor. The values of R1 and R2 are 10k Ω and 10 Ω respectively. The decoupling capacitor,

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C1, on the VPD line is 1000 pF.

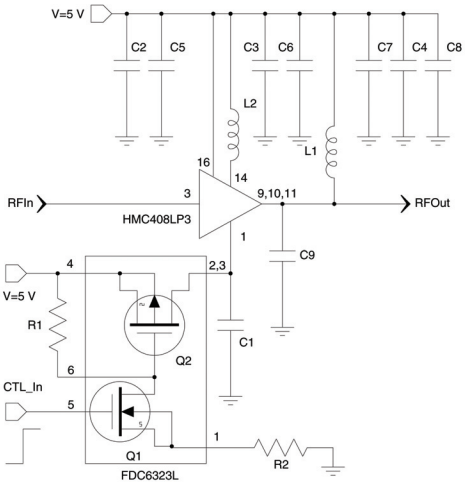


**Figure 2** - HMC408LP3 with integrated load switch

A DC analysis using =HARBEC=[2] is performed to determine the current usage of the load switch. The load presented at the VPD pin is determined by measuring the current at different VPD voltages and then applying ohms law to determine the equivalent resistance. The values are plotted and then the curve is fitted using a 3rd order polynomial as shown in equation (2). Equation (2) is then used in the simulation to determine the load resistance as a function of VPD.

$$R_{laod} = 9382.4 - 5980.4 \cdot VPD + 1327.7 \cdot VPD^2 - 98.511 \cdot VPD^3 \quad (2)$$

Figure 3 shows the measured and calculated ( using equation (2)) values of the load resistance versus VPD voltage. The calculated data is a ”good” fit to the measured data.

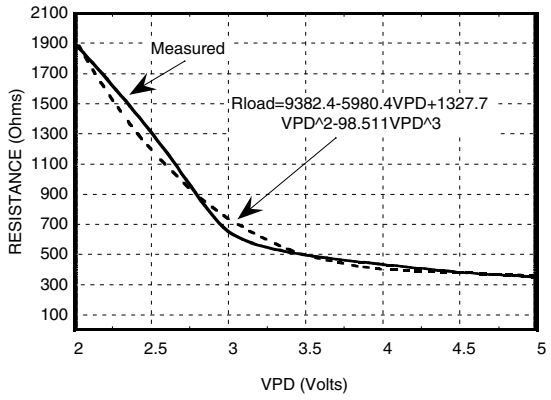


**Figure 3 -** Load resistance versus VPD voltage

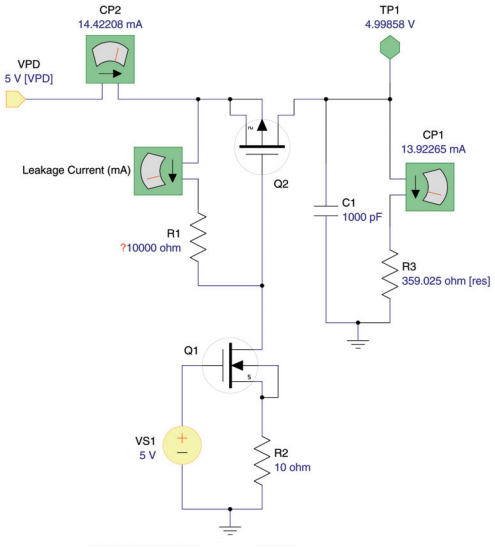


**Figure 4**- Model for load switch

Figure 4 shows the =HARBEC= model used for the load switch. The parameters for MOSFET devices are obtained from the Fairchild website. The load resistor R3 varies as a function of the input voltage VPD, which is expressed by equation (2). Resistor R1 is the pull up resistor, which is used to turn off Q2. R2 dampens the current during turn on while C1 is the decoupling capacitor located at the input of the VPD pin.

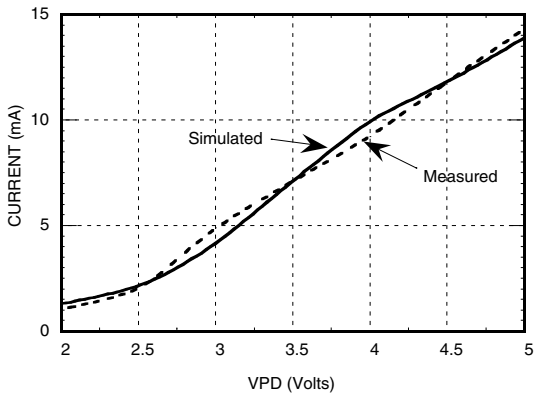


**Figure 5**- Current into VPD pin

The simulation shows that a logic “low” applied to the gate of Q1 shuts off the switch and power amplifier by cutting off the current to the VPD pin. Applying a logic “high” to the gate of Q1 turns the load switch on resulting in a positive voltage being applied to

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the VPD pin of the amplifier. Figure 5 compares the measured load current to the simulated versus VPD voltage.

Figure 6 shows the leakage current through R1, Q2, and R2 to ground. As seen in the figure, leakage current increases with lower values of R1.

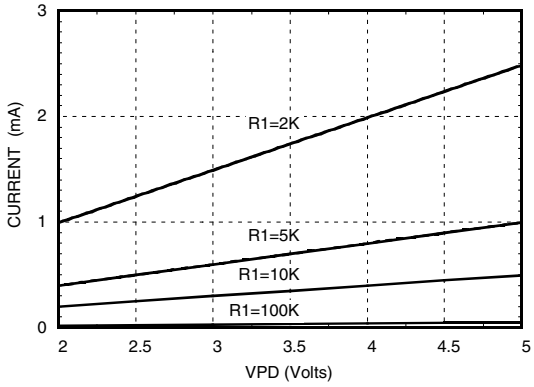


**Figure 6** - Leakage current versus R1

## *Limitations and Trade-offs*

The amplifier is initially tested to assure that the load switch has no adverse effects on performance (excluding rise / fall time). Rise / fall time are then measured using the test set up described in figure 7 which utilizes a wide bandwidth oscilloscope.

With the value of R2 set to 10 Ω and R1 to 10 kΩ, the fall time is measured to be 4.6 μS and the rise time is 71.0 nS as shown in figure 8a and 8b respectively. The leakage current is simulated to be 0.5 mA as shown in figure 6.

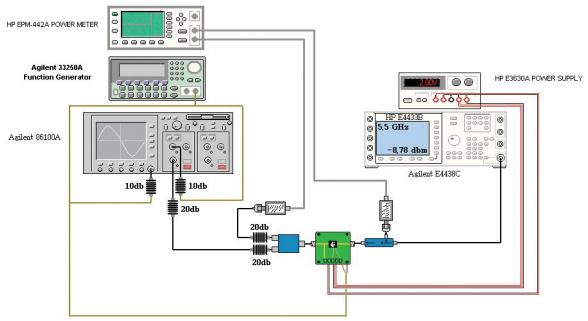


**Figure 7-** Rise/Fall time measurement set-up

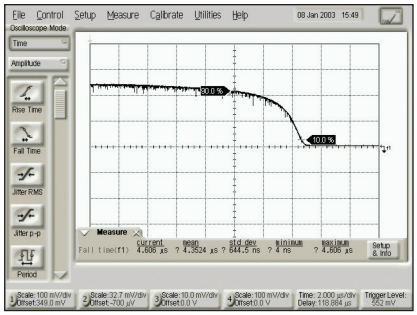

**Figure 8** - (a) Fall time

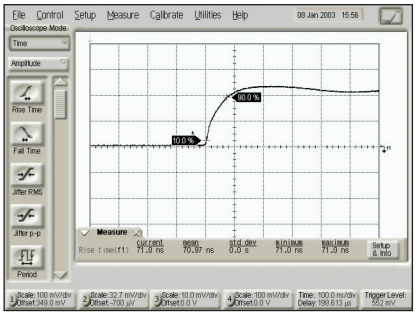

**Figure 8** - (b) Rise time

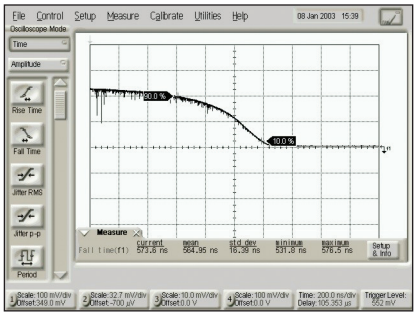

**Figure 9** - (a) Fall time

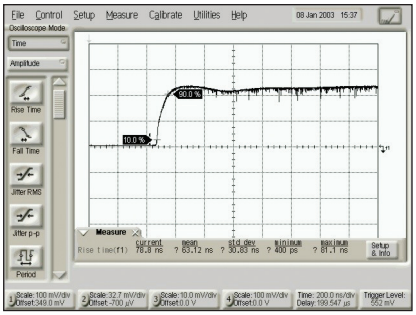

**Figure 9** - (b) Rise time



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In order to reduce the fall time, resistor R1 is reduced from 10 kΩ to 2 kΩ. R2 is not changed since little or no improvement can be made to the rise time. The reduction in R1 decreased the fall time from 4.6 μS to 573 nS as shown in figure 9a. However, due to the decrease in R2 the leakage current has increased to 2.5 mA as shown in figure 6. The rise time is relatively unchanged as shown in figure 9b.

## Conclusion

A simple, low cost, CMOS power control circuit is implemented to power down the HMC408LP3 power amplifier. The circuit allows power down for a variety of logic families while maintaining performance of the amplifier with the exception of rise and fall time. It is shown that fall time may be improved at the expense of leakage current through the load switch. This load switch may be adapted to the entire family of Hittite amplifiers that utilize power control (See table 1). The circuit is realized using either discrete MOSFET devices or an integrated dual MOSFET IC.

| Part Number | VPD (V) | IPD (mA) |
|---|---|---|
| HMC314 | 5 | 12 |
| HMC326MS8G | 5 | 7 |
| HMC327MS8G | 5 | 7 |
| HMC406MS8G | 5 | 7 |
| HMC407MS8G | 5 | 7 |
| HMC408LP3 | 5 | 14 |
| HMC413QS16G | 3.6 | 7 |
| HMC414MS8G | 3.6 | 7 |
| HMC415LP3 | 3 | 7 |

**Table 1**- Hittite amplifiers with power control

**(Endnotes)**

[1] The author recognizes that there are logic circuits on the market that are capable of meeting the 14mA requirement.

[2] =HARBEC=, Harmonic Balance Simulator, Eagleware Corporation, Norcross, GA.